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(54) **ORGANIC LIGHT EMITTING DISPLAY DEVICE**
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(57) **ABSTRACT**

An organic light emitting display device can include an organic light emitting diode (OLED), a driving transistor connected to an anode electrode of the OLED, a scan transistor, a digital-to-analog converter (DAC) and a sensing unit. The scan transistor is connected the anode electrode of the OLED and a data line. The DAC supplies a data voltage for displaying to the data line in a displaying period and supplies a data voltage for sensing to the data line in a sensing period. The sensing unit obtains an anode voltage of the OLED as a sensing voltage through the data line in the sensing period.

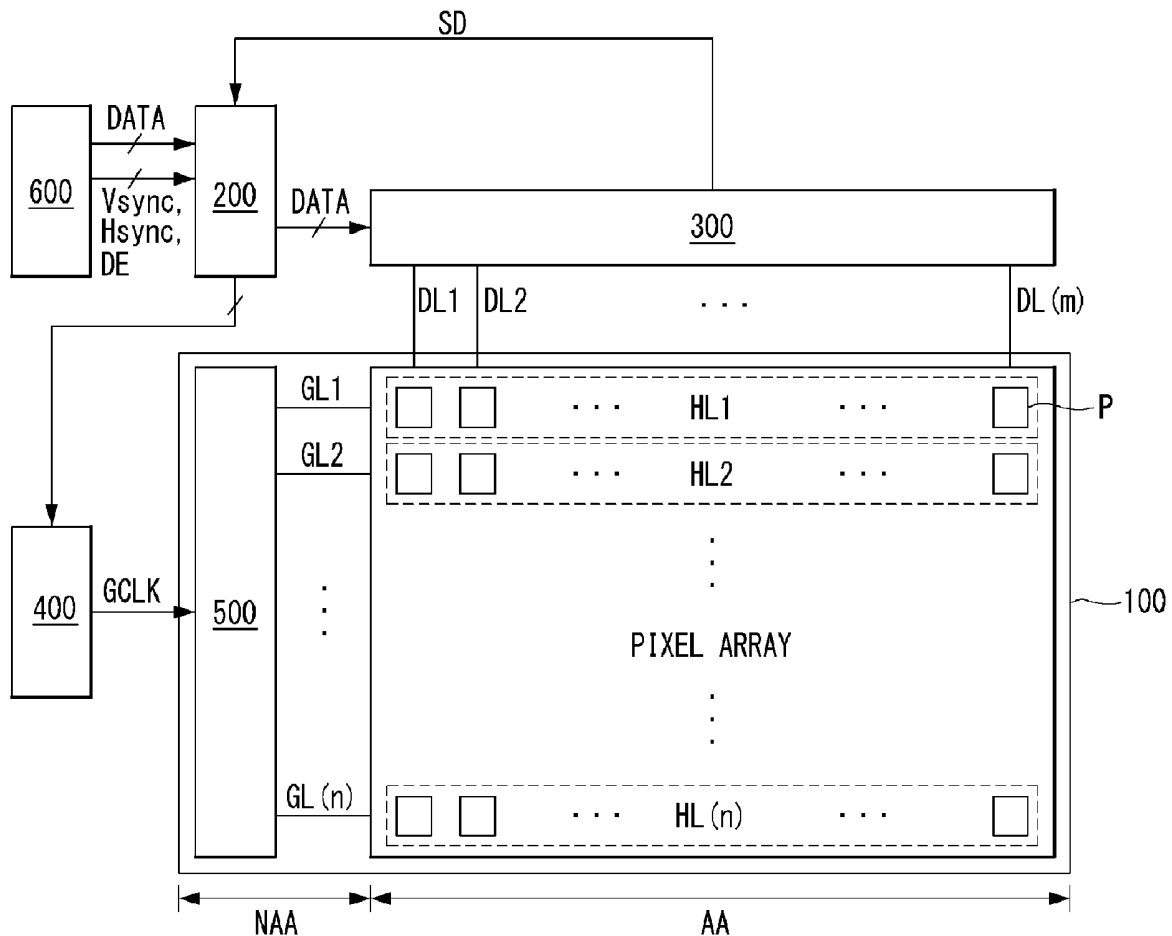


FIG. 1

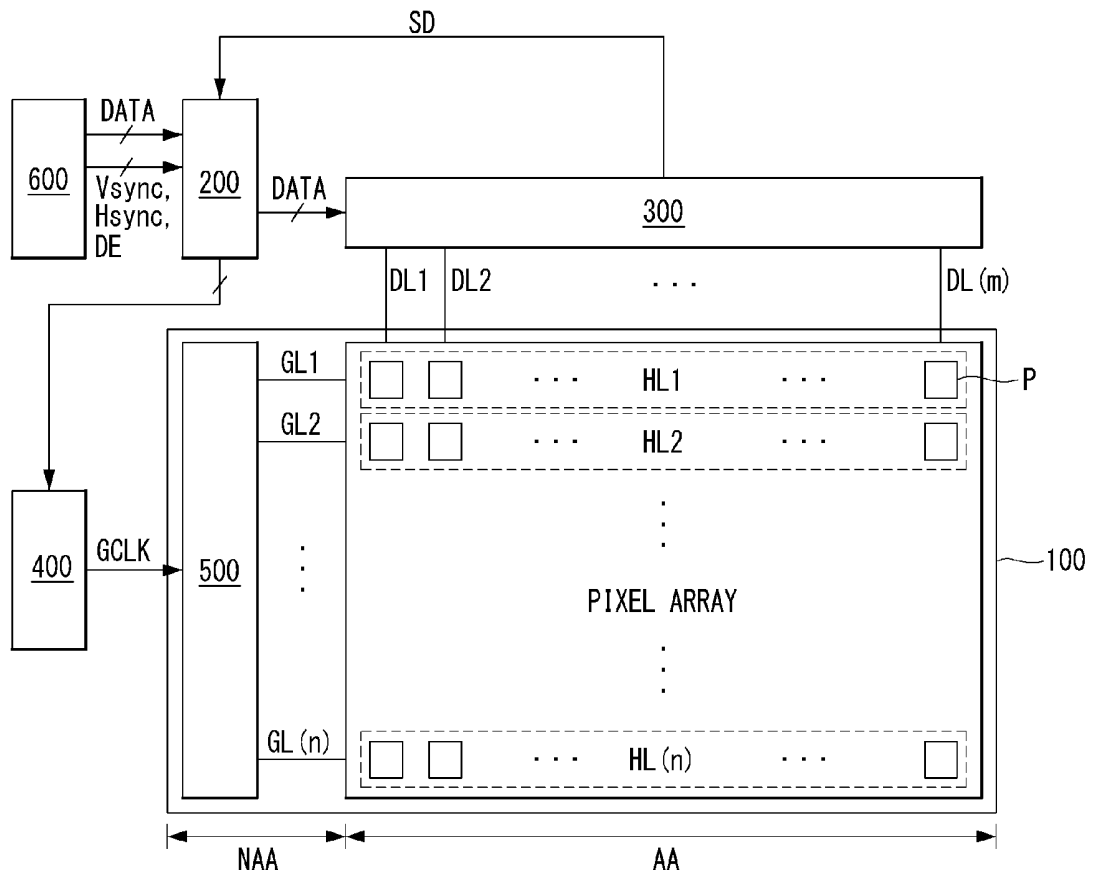


FIG. 2

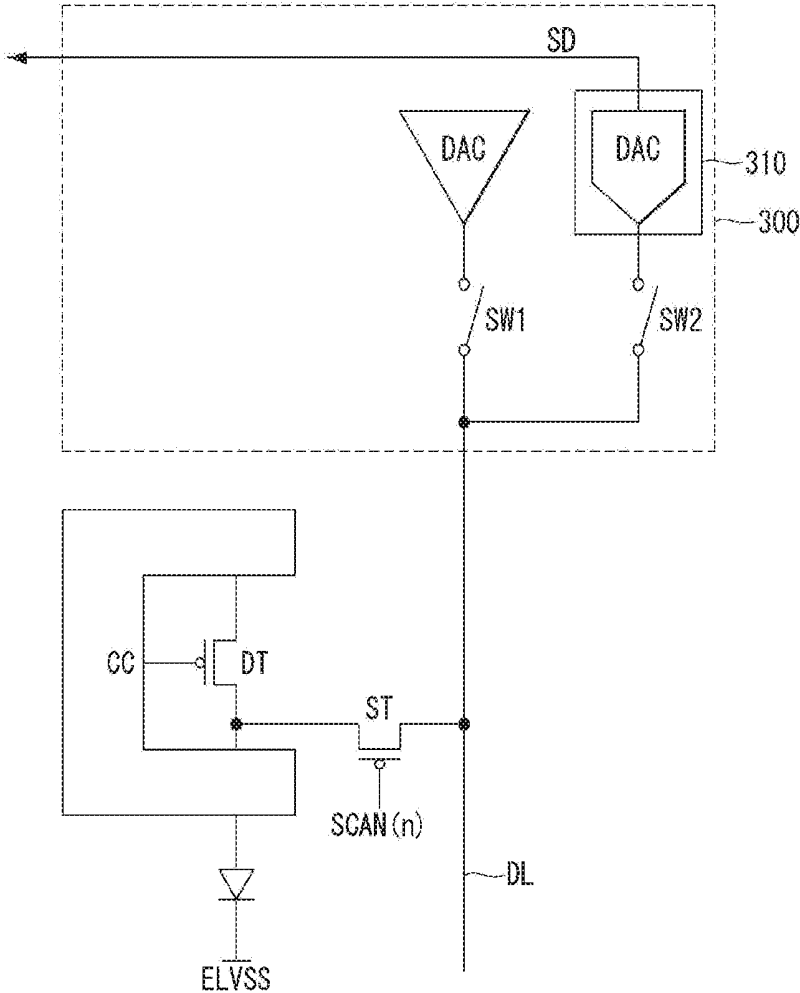


FIG. 3

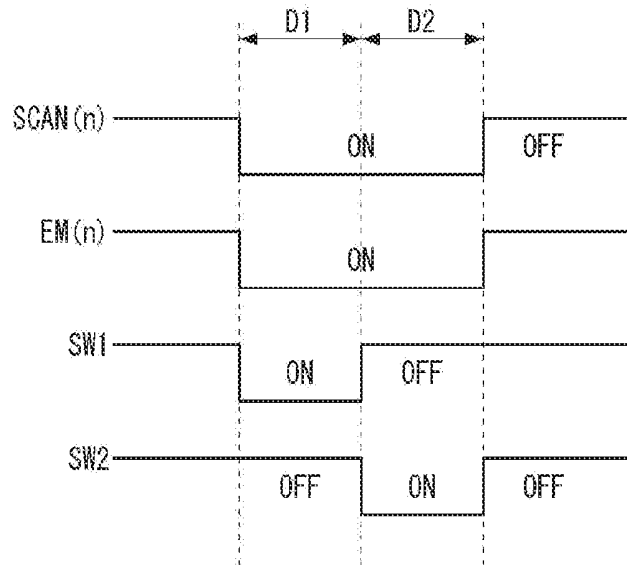


FIG. 4

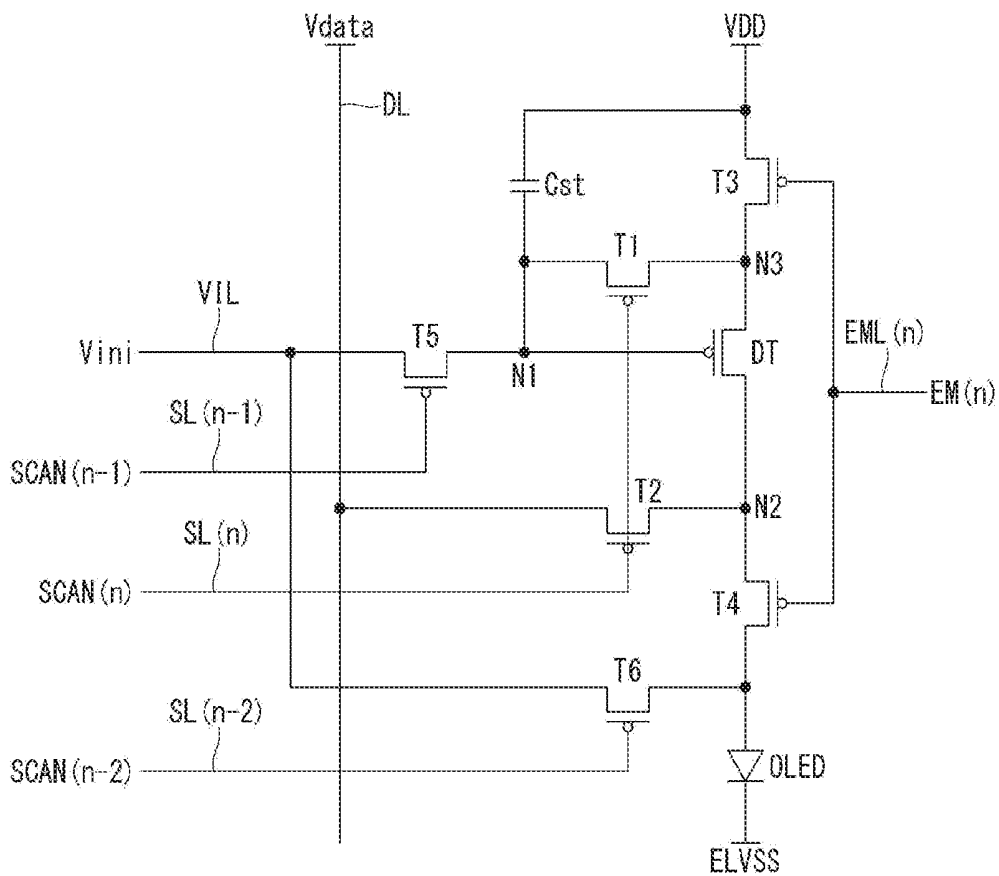


FIG. 5

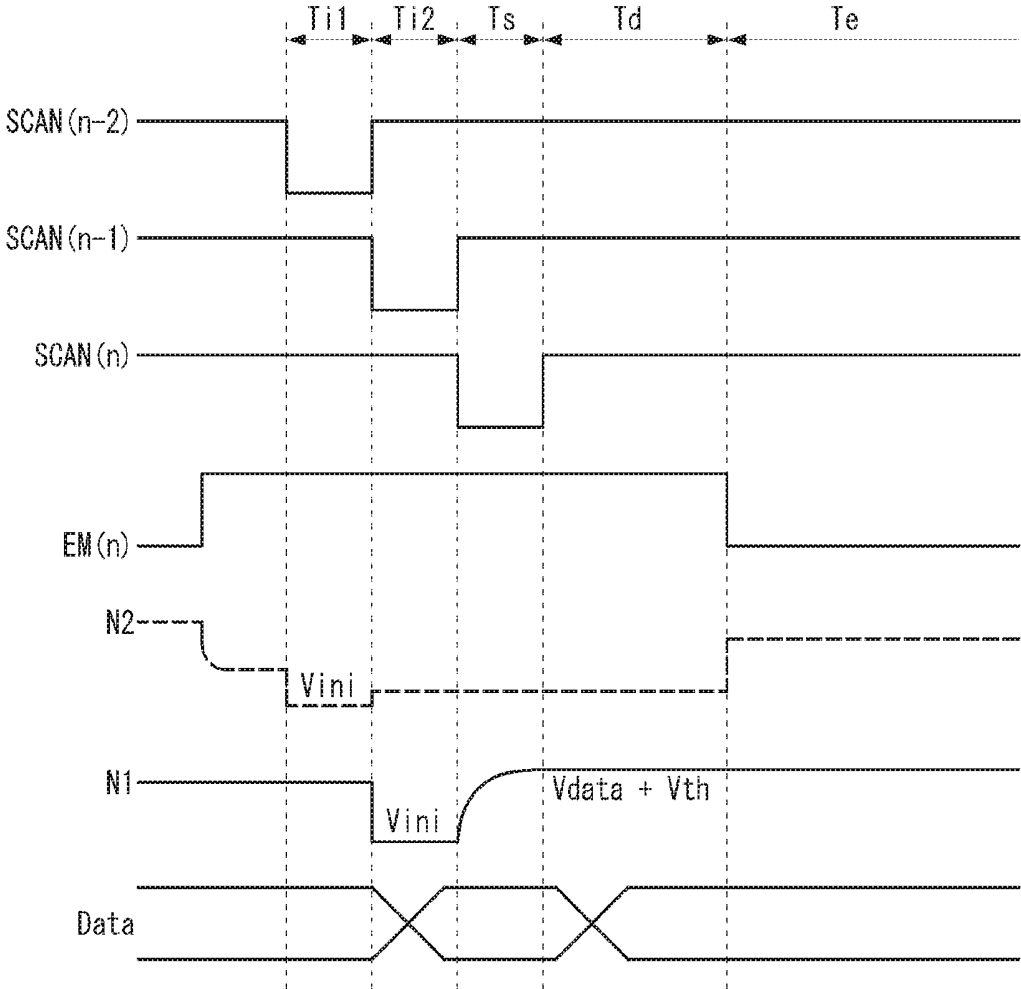


FIG. 6A

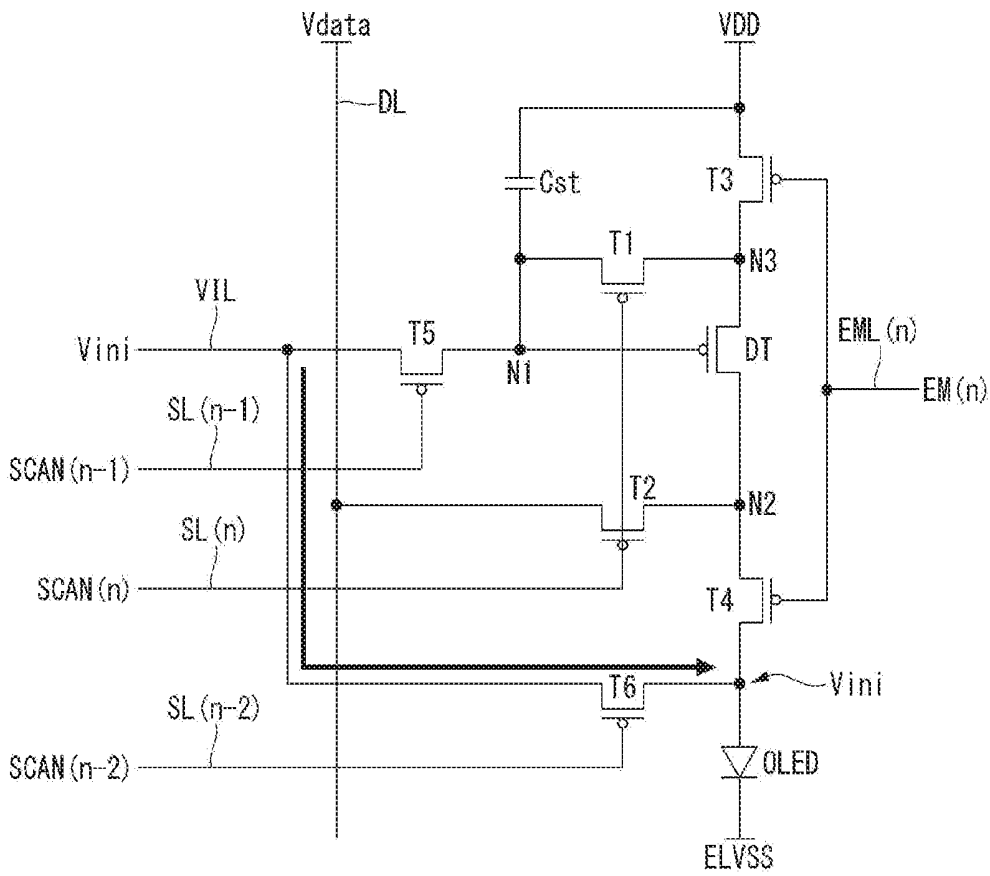


FIG. 6B

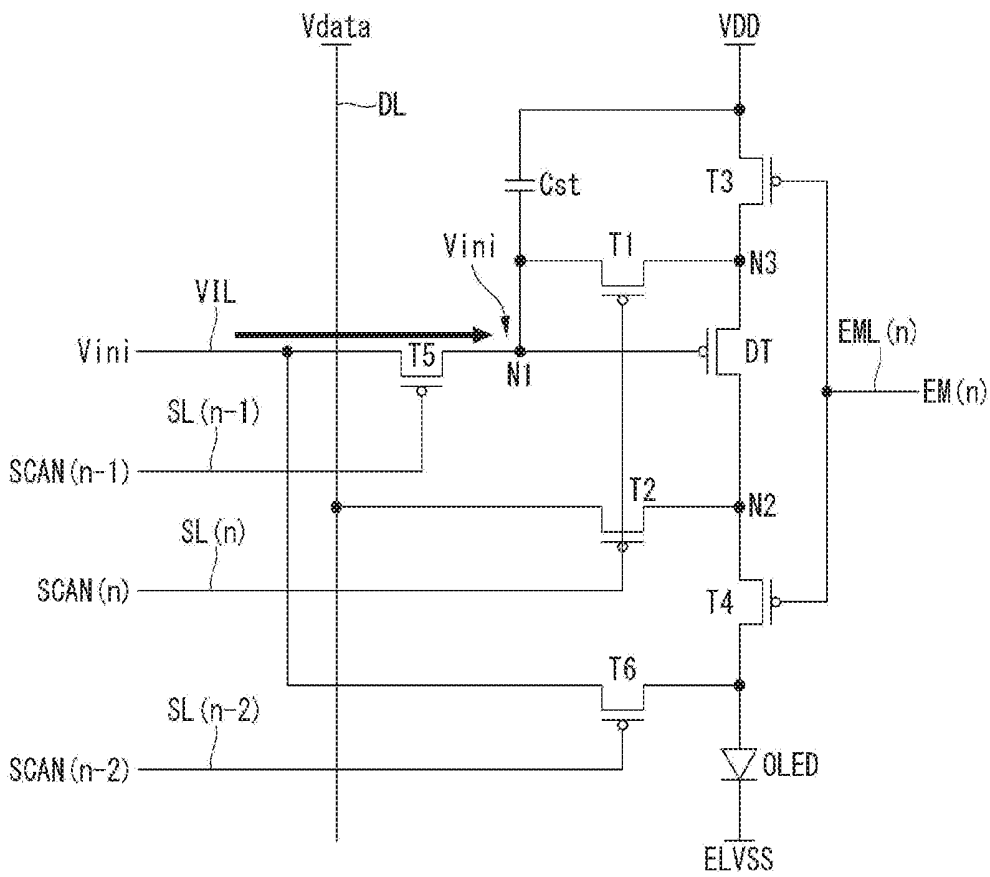


FIG. 6C

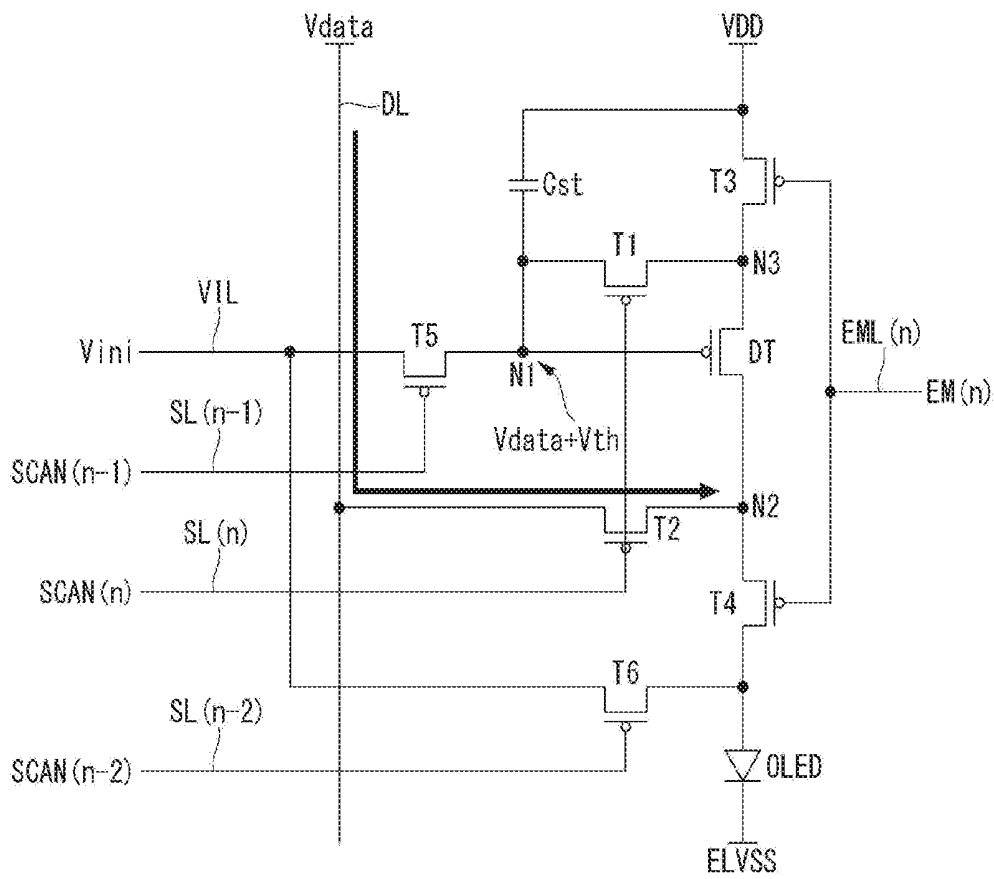


FIG. 6D

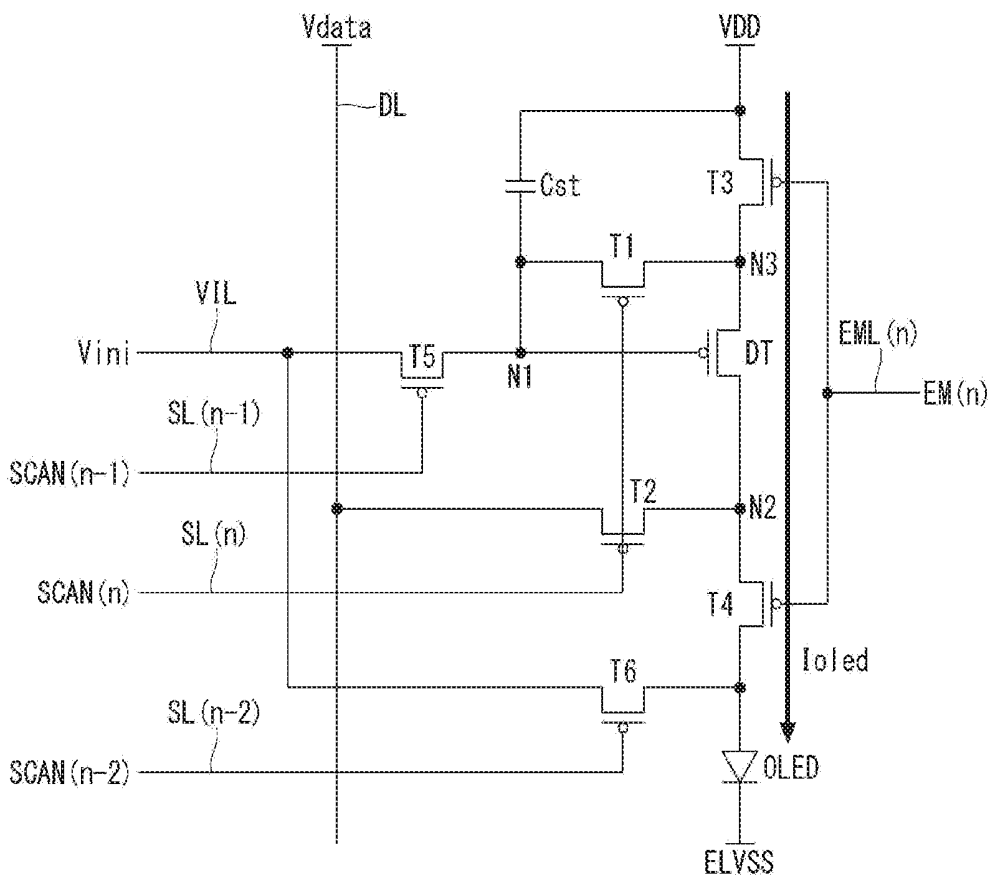


FIG. 7

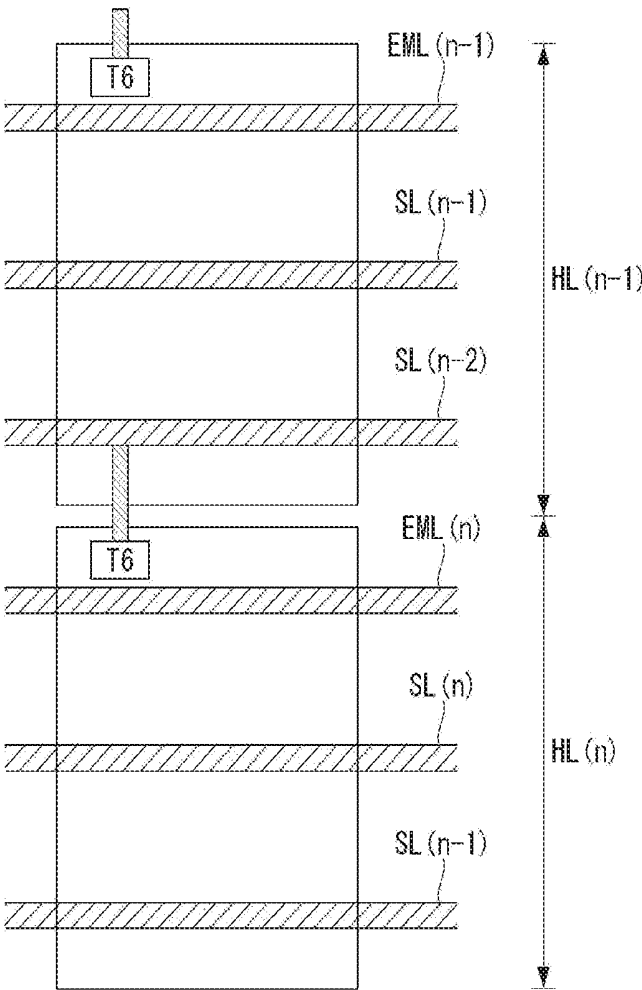


FIG. 8

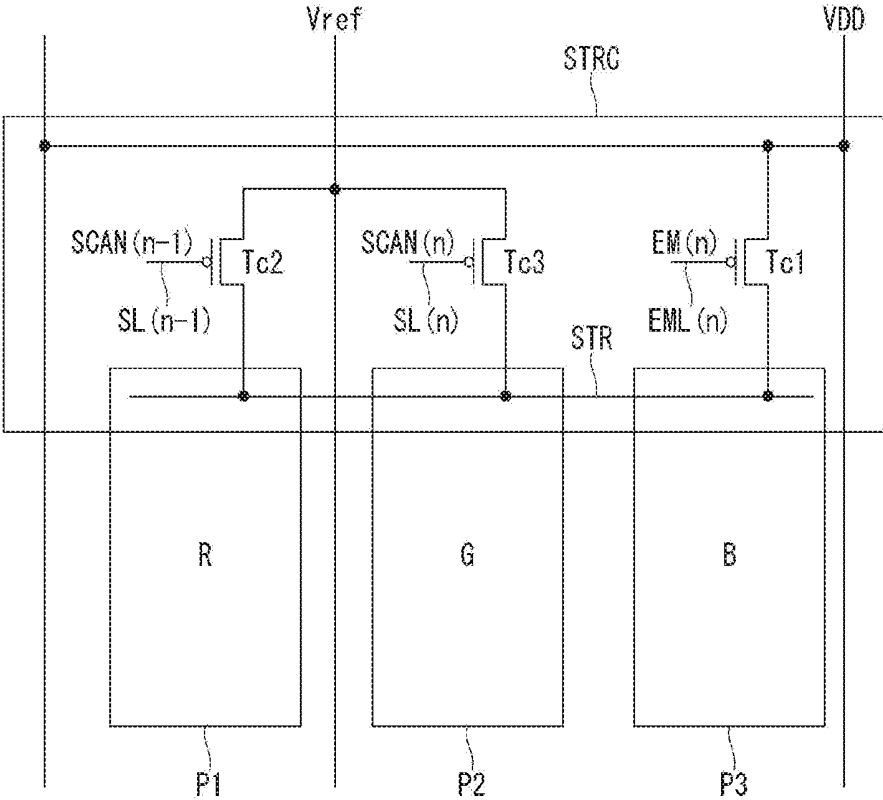


FIG. 9

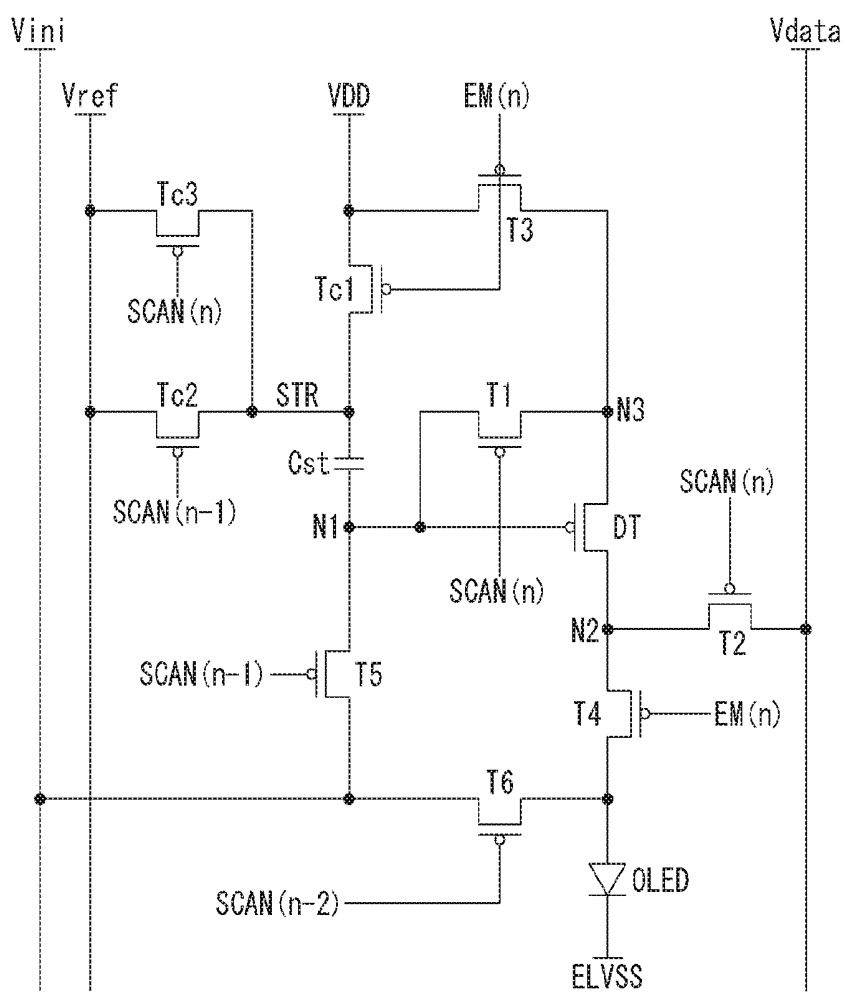


FIG. 10

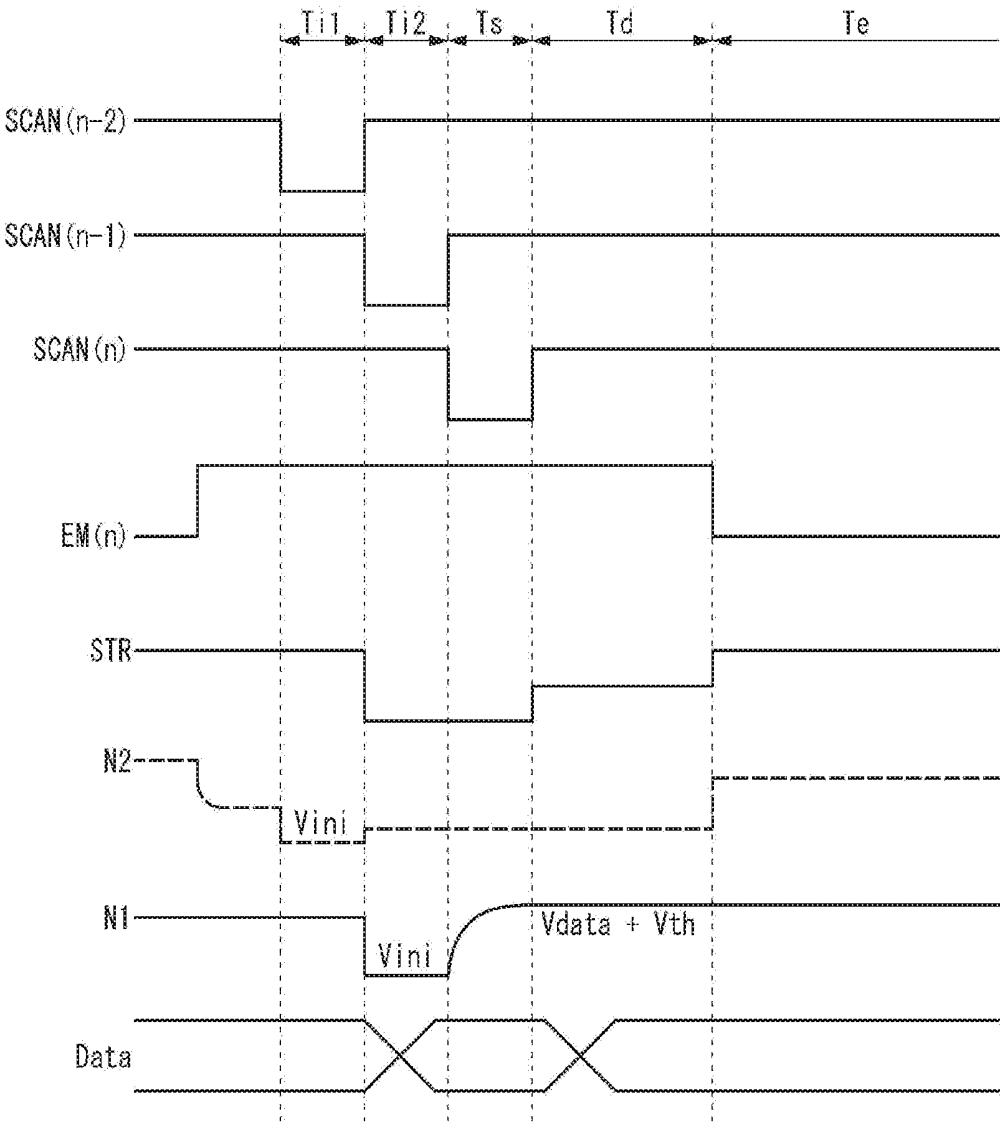


FIG. 11A

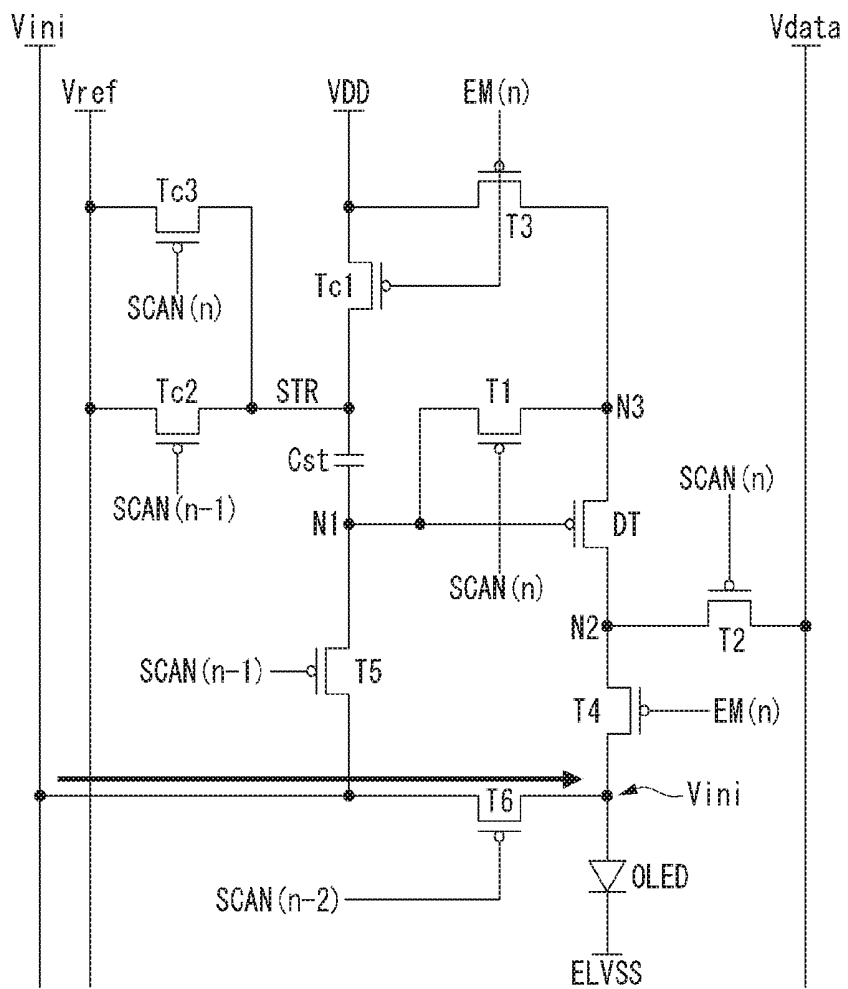


FIG. 11B

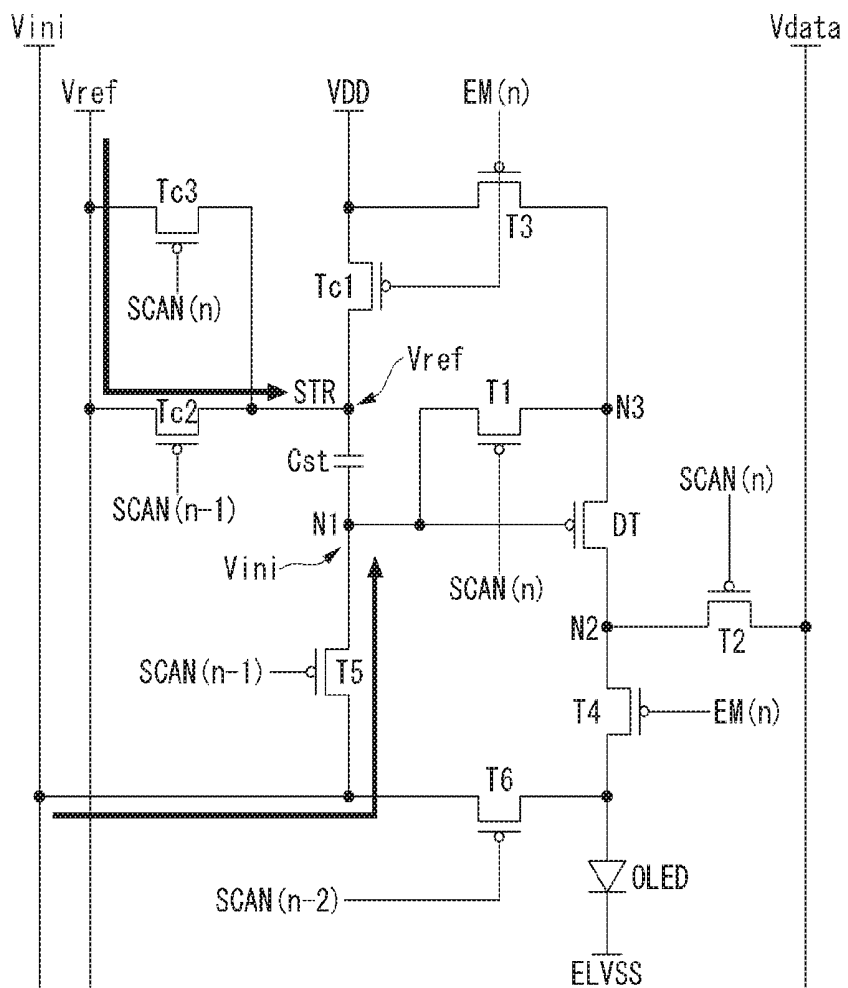
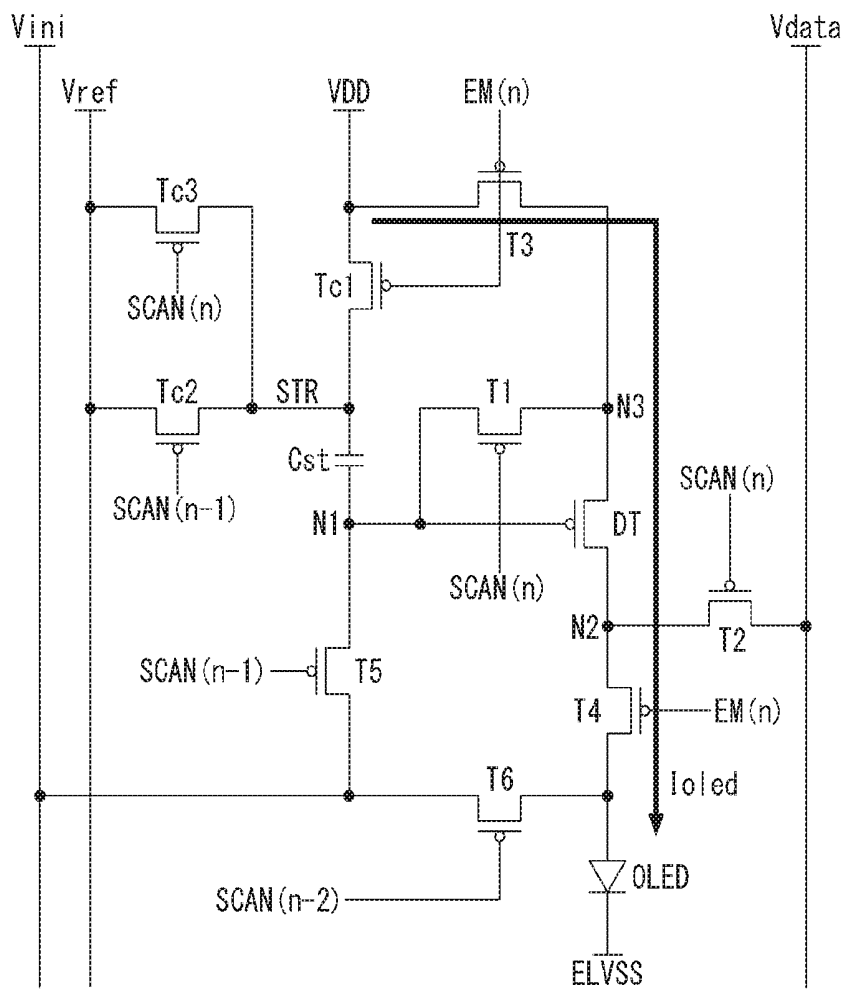


FIG. 11D



ORGANIC LIGHT EMITTING DISPLAY DEVICE

[0001] This application claims the priority benefit of Korean Patent Application No. 10-2018-0138090 filed on Nov. 12, 2018 in the Republic of Korea, which is incorporated herein by reference for all purposes as if fully set forth herein.

BACKGROUND

Field

[0002] The present disclosure relates to an organic light emitting display device of an active matrix type.

Discussion of the Related Art

[0003] The organic light emitting display device of an active matrix type includes an organic light emitting diode (OLED) emitting light itself, and is advantageous in that response speed, luminous efficiency and luminance are high, and viewing angle is large.

[0004] The OLED which is a self light-emitting element includes anode and cathode electrodes and an organic compound layer formed therebetween. The organic compound layer comprises a hole injection layer, a hole transport layer, an emission layer, an electron transport layer, and an electron injection layer. When driving voltages are applied to the anode and cathode electrodes, the holes passing the hole transport layer and the electrons passing the electron transport layer move to form excitons, which causes the emission layer to emit visible light.

[0005] In the organic light emitting display device, pixels each including the OLED and a driving transistor are arranged in a matrix form, and control the luminance of input image according to the gray scale of image data. The driving transistor controls the driving current flowing through the OLED according to the potential difference between the gate and source electrodes of the driving transistor. The amount of the light emitted by the OLED is determined by the driving current, and image luminance is determined by the light amount emitted by the OLED.

[0006] The OLED is deteriorated as an emission time of the OLED increases. If the OLED is deteriorated, the threshold voltage capable of turning on the OLED increases and emission efficiency decreases. Since the cumulative emission time of the OLED can be different for each pixel, the deterioration of the OLED can be different for each pixel. The difference in the deterioration of the OLEDs between the pixels can cause a luminance variation and can result in image sticking phenomenon.

[0007] Accordingly, a deterioration compensation technique which determines whether the OLED is deteriorated by sensing the threshold voltage of the OLED and corrects image data with a compensation gain that can compensate for the deterioration of OLED has been used. In this regard, in order to simplify a pixel structure and realize a high-resolution display panel, it is necessary to simplify the structure for sensing the threshold voltage of the OLED.

SUMMARY

[0008] Therefore, it is an objective of the present disclosure to provide an organic light emitting display device

which is advantageous in realizing a high resolution by simplifying a structure for sensing a threshold voltage of an organic light emitting diode.

[0009] The organic light emitting display device of the present disclosure can comprise an organic light emitting diode (OLED), a driving transistor connected to an anode electrode of the OLED, a scan transistor, a digital-to-analog converter (DAC) and a sensing unit. The scan transistor is connected the anode electrode of the OLED and a data line. The DAC supplies a data voltage for displaying to the data line in a displaying period and supplies a data voltage for sensing to the data line in a sensing period. The sensing unit obtains an anode voltage of the OLED as a sensing voltage through the data line in the sensing period.

[0010] Since the organic light emitting diode display device according to the present disclosure does not require additional patterns and switch elements and performs a sensing operation using only the configuration of an internal compensation circuit necessary during a displaying period, the pixel structure can be simplified.

[0011] Since a sensing voltage is obtained by using a data line, an initialization line can be disposed as a horizontal line. As a result, the design margin can be increased, which is advantageous in realizing a high resolution.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The accompanying drawings, which are included to provide a further understanding of the disclosure and are incorporated in and constitute a part of this specification, illustrate embodiments of the disclosure and together with the description serve to explain the principles of the disclosure. In the drawings:

[0013] FIG. 1 is a view illustrating an organic light emitting display device according to an embodiment of the present disclosure.

[0014] FIG. 2 illustrates a pixel circuit and a data driver according to the present disclosure.

[0015] FIG. 3 is a diagram illustrating the operation of switch elements in a sensing period.

[0016] FIG. 4 is a diagram showing a pixel circuit according to a first embodiment of the present disclosure.

[0017] FIG. 5 is a diagram illustrating the operation timings of driving signals and the voltage changes of main nodes according to the first embodiment of the present disclosure.

[0018] FIGS. 6A to 6D are views for explaining the operations of the first pixel circuit in an image displaying period.

[0019] FIG. 7 is a schematic diagram of pixels according to the first embodiment of the present disclosure.

[0020] FIG. 8 is a diagram showing an array structure of pixels according to a second embodiment of the present disclosure.

[0021] FIG. 9 is a diagram showing a pixel circuit according to the second embodiment of the present disclosure.

[0022] FIG. 10 is a diagram illustrating the operation timings of driving signals and the voltage changes of main nodes according to the first embodiment of the present disclosure.

[0023] FIGS. 11A to 11D are views for explaining the operations of the second pixel circuit in an image displaying period.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0024] Hereinafter, preferred embodiments of the present disclosure will be described in detail with reference to the accompanying drawings. The same reference numerals throughout the specification denote substantially identical components. In the following description, a detailed description of known functions and configurations incorporated herein will be omitted when it can make the subject matter of the present disclosure rather unclear.

[0025] Hereinafter, embodiments of the present disclosure will be described with reference to the drawings.

[0026] FIG. 1 is a view illustrating an organic light emitting display device according to an embodiment of the present disclosure. All the components of the organic light emitting display device according to all embodiments of the present disclosure are operatively coupled and configured.

[0027] Referring to FIG. 1, the organic light emitting display device according to an embodiment of the present disclosure includes a display panel 100, a data driver 300, gate drivers 400 and 500, and a timing controller 200.

[0028] In a display area AA of the display panel 100, a plurality of data lines DL1 to DLm and a plurality of gate lines GL1 to GLn cross each other, and pixels P are arranged in a matrix form. Each of pixel lines HL1 to HLn includes pixels arranged in a same row. When the number of the pixels P arranged in the display area AA is $m \times n$, the display area AA includes n pixel lines. Herein, each of the pixels P refers to either a red subpixel, a green subpixel or a blue subpixel for color implementation, or can be another type such as a white subpixel. Each of the pixels P is supplied with a high-potential voltage VDD and a low-potential voltage ELVSS from a power generating unit. The pixels P arranged in a first pixel line HL1 are connected to a first gate line GL1 and the pixels P arranged in an n-th pixel line HLn are connected to an n-th gate line GLn. The gate lines GL1 to GLn can include a plurality of lines for providing respective gate signals.

[0029] The timing controller 200 generates data control signals for controlling the operation timing of the data driver 300 and gate control signals for controlling the operation timings of the gate drivers 400 and 500 based on timing signals such as a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, and a data enable signal DE supplied from a host 600.

[0030] The timing controller 200 generates a compensation value for compensating for a variation in deterioration of organic light emitting diodes OLEDs based on the sensing data SD provided from the data driver 300 in a sensing period. And the timing controller can correct image data based on the compensation value.

[0031] The data driver 300 supplies the data voltage for sensing to the pixels P, converts the sensing voltage input through the data line DL to a digital value and supplies it to the timing controller 200, during the sensing period. The data driver 300 supplies a data voltage for displaying to the data line DL during a displaying period.

[0032] The gate driver includes a level shifter 400 and a shift register 500. The level shifter 400 generates gate clocks GCLK based on the gate control signal provided from the timing controller 200. The shift register 500 outputs gate pulses based on the gate clocks GCLK output from the level shifter 500. To this end, the shift register 500 includes shift registers which are connected to each other in a dependent

manner. The shift register 500 can be formed directly on a non-display area NAA of the display panel 100 in accordance with a gate-driver in panel GIP scheme.

[0033] FIG. 2 illustrates an example of a pixel circuit and a data driver usable in the organic light emitting display device of FIG. 1 according to the present disclosure, and FIG. 3 is a diagram illustrating the operation timings of a scan transistor and first and second switch elements in a sensing period.

[0034] Referring to FIGS. 2 and 3, the pixel (e.g., P in FIG. 1) according to an embodiment of the present disclosure comprises an OLED, a driving transistor DT, a scan transistor Ts and a compensation circuit CC.

[0035] The OLED includes an organic compound layer positioned between an anode electrode and a cathode electrode. The driving transistor DT controls the driving current applied to the OLED according to its source-gate voltage Vsg. The scan transistor ST connects the anode electrode of the OLED and the data line DL in response to a scan signal SCAN(n). The data driver 300 includes a digital-to-analog converter DAC and a sensing unit 310. The DAC converts image data DATA into an analog-type data voltage to generate a data voltage Vdata.

[0036] The sensing unit 310 acquires the anode voltage of the OLED as a sensing voltage during a sensing period. The sensing unit 310 includes an analog-to-digital converter ADC for converting the sensing voltage into sensing data SD of a digital form.

[0037] A first switch SW1 selectively connects the DAC and the data line DL. The first switch SW1 maintains its turn-on state to provide the data voltage Vdata output from the DAC to the data line DL during the displaying period for displaying image. The first switch SW1 maintains its turn-on state to provide the data voltage Vdata output from the DAC to the data line DL during a first period D1 of the sensing period. The data voltage Vdata output by the DAC during the first period D1 of the sensing period corresponds to the data voltage for sensing.

[0038] A second switch SW2 selectively connects the ADC and the data line DL. The second switch SW2 is turned on to acquire the anode voltage of the OLED as the sensing voltage during a second period D2 within the sensing period.

[0039] The sensing period is a period during which a sensing operation is performed for sensing a threshold voltage of the OLED and compensating for a threshold voltage deviation of respective pixels. The sensing period can be included in a predetermined driving preparation period from when the display device is turned on or can be included in a period before the power is completely turned off by a power off signal.

[0040] Hereinafter, specific embodiments of the present disclosure will be described.

[0041] FIG. 4 is a diagram showing a pixel circuit according to a first embodiment of the present disclosure.

[0042] Referring to FIG. 4, the pixel (e.g., P in FIG. 1) according to the first embodiment includes an OLED, a driving transistor DT, a first transistor T1, a scan transistor T2, first and second emission control transistors T4 and T3, first and second initialization transistors T5 and T6 and a storage capacitor Cst.

[0043] The driving transistor DT controls the driving current applied to the OLED according to its source-gate voltage Vsg. In the driving transistor DT, a gate electrode is connected to a first node N1, a drain electrode is connected

to a second node N2, and a source electrode is connected to the input terminal of a high potential voltage VDD through the second emission control transistor T3.

[0044] The first transistor T1 includes a gate electrode connected to an n-th scan line SL(n), a source electrode connected to a third node N3, and a drain electrode connected to the first node N1. The first transistor T1 connects the gate electrode and the drain electrode of the driving transistor DT in response to an n-th scan signal SCAN(n).

[0045] The scan transistor T2 (hereinafter referred to as a second transistor) includes a gate electrode connected to the n-th scan line SL(n), a source electrode connected to the data line DL, and a drain electrode connected to the second node N2. The second transistor T2 connects the data line DL and the second node N2 in response to the n-th scan signal SCAN(n).

[0046] The first emission control transistor T4 (hereinafter referred to as a fourth transistor) includes a gate electrode connected to an n-th emission line EML(n), a source electrode connected to the second node N2, and a drain electrode connected to an anode electrode of the OLED. The fourth transistor T4 connects the anode electrode of the OLED with the second node N2 in response to the n-th emission signal EM(n).

[0047] The second emission control transistor T3 (hereinafter referred to as a third transistor) includes a gate electrode connected to the n-th emission line EML(n), a source electrode connected to the input terminal of the high potential voltage VDD, and a drain electrode connected to the third node N3. The third transistor T3 applies the high potential voltage VDD to the third node N3 in response to the n-th emission signal EM(n).

[0048] The first initialization transistor T6 (hereinafter, referred to as a sixth transistor) includes a gate electrode connected to an (n-2)-th scan line SL(n-2), a source connected to the anode of the OLED, and a drain electrode connected to an initialization line VIL. The sixth transistor T6 applies an initialization voltage Vini to the anode of the OLED in response to an (n-2)-th scan signal SCAN(n-2).

[0049] The second initialization transistor T5 (hereinafter, referred to as a fifth transistor) includes a gate electrode connected to an (n-1)-th scan line SL(n-1), a source connected to the first node N1, and a drain electrode connected to the initialization line VIL. The fifth transistor T5 applies the initialization voltage Vini to the first node N1 in response to an (n-1)-th scan signal SCAN(n-1).

[0050] The storage capacitor Cst includes a first electrode connected to the input terminal of the high potential voltage VDD and a second electrode connected to the first node N1.

[0051] The pixel circuit according to the first embodiment compensates the change of the threshold voltage of the driving transistor DT in real time within the displaying period according to an internal compensation scheme.

[0052] FIG. 5 is a diagram illustrating the timings of gate signals in the displaying period according to the first embodiment, and FIGS. 6A to 6D are equivalent circuit diagrams of pixels in a first initialization period, a second initialization period, a sampling period, and a light emission period, respectively.

[0053] Referring to FIGS. 4 to 6D, the operations of the pixel is as follows which emits light while compensating for the threshold voltage change of the driving transistor in real time.

[0054] Referring to FIGS. 4, 5 and 6A, in the first initialization period Ti1, the (n-2)-th scan signal SCAN(n-2) maintains a turn-on voltage. The sixth transistor T6 applies the initialization voltage Vini to the anode of the OLED in response to the (n-2)-th scan signal SCAN(n-2). As a result, the anode of the OLED is initialized to the initialization voltage Vini in the first initializing period Ti1. The initialization voltage Vini is selected within a voltage range sufficiently lower than the operation voltage of the OLED and can be set to be equal to or lower than the low potential voltage ELVSS.

[0055] Referring to FIGS. 4, 5 and 6B, the (n-1)-th scan signal SCAN(n-1) maintains the turn-on voltage in the second initialization period Ti2. The fifth transistor T5 applies the initialization voltage Vini to the first node N1. In the second initializing period Ti2, the first node N1 is initialized to the initialization voltage Vini.

[0056] Referring to FIGS. 4, 5 and 6C, in the sampling period Ts, the n-th scan signal SCAN(n) maintains the turn-on voltage. The first transistor T1 connects the first node N1 and the third node N3 in response to the n-th scan signal SCAN(n). The second transistor T2 writes a data voltage Vdata to the second node N2 in response to the n-th scan signal SCAN(n). A current flows between the drain and source electrodes of the driving transistor DT in the sampling period Ts, and this current flows until the voltage of the source electrode is saturated to the magnitude of the sum (Vdata+Vth) of the data voltage Vdata and the threshold voltage Vth of the driving transistor DT. That is, during the sampling period Ts, the gate electrode of the driving transistor DT is sampled with a magnitude of (Vdata+Vth).

[0057] Referring to FIGS. 4, 5 and 6D, in the sampling period Ts, the n-th emission signal EM(n) maintains the turn-on voltage in the emission period Te after a holding period Td. The third transistor T3 and the fourth transistor T4 are turned on in response to the n-th emission signal EM(n), and as a result, a current is generated from the input terminal of the high potential voltage VDD to the anode of the OLED depending on the voltage set between the gate and the source of the driving transistor DT.

[0058] The driving current Ioled flowing in the OLED in the emission period Te is as shown in the following Equation 1.

$$I_{oled} = k/2 \left\{ (V_{gs} - V_{th}) \right\}^2 = k/2 \left\{ (V_g - V_s - V_{th}) \right\}^2 = k/2 \left\{ (V_{data} + V_{th}) - V_{DD} - V_{th} \right\}^2 \quad \text{Equation 1}$$

[0059] At this time, since $V_{th} < 0$, Equation 1 becomes $k/2 \{ (V_{data} - V_{DD}) \}^2$.

[0060] In Equation 1, k represents a proportional constant determined by electron mobility, parasitic capacitance, and channel capacitance of the driving transistor DT, and the like. As a result, during the light emission period Te, the driving current flowing through the OLED is not affected by the threshold voltage Vth of the driving transistor DT.

[0061] The pixel circuit according to the first embodiment compensates for the threshold voltage deviation of the OLED within the sensing period.

[0062] Referring to FIGS. 2, 3 and 5, the process of sensing the threshold voltage of the OLED in the pixel circuit according to the first embodiment will be described.

[0063] During the first period D1 to the second period D2, the second transistor T2 maintains a turn-on state in response to the n-th scan signal SCAN(n), and the fourth transistor T4 maintain the turn-on state in response to the n-th emission signal EM(n).

[0064] During the first period D 1, the first switch SW1 is turned on and the data line DL is connected to the DAC of the data driver 300. The data driver 300 outputs the data voltage for sensing through the DAC. The data voltage for sensing is set to a voltage value sufficiently higher than the threshold voltage of the OLED.

[0065] The data voltage for sensing Vdata output from the DAC is applied to the anode of the OLED via the second transistor T2 and the fourth transistor T4.

[0066] During the second period D2, the second switch SW2 is turned on, and the data line DL is connected to the ADC. In the second period D2, the OLED emits light, and the anode voltage of the OLED gradually decreases because it is discharged through OLED. The anode voltage of the OLED is discharged until it reaches the threshold voltage of the OLED. The ADC senses the threshold voltage of the OLED through the data line DL.

[0067] As described above, the organic light emitting display device according to the first embodiment senses the threshold voltage of the OLED through the data line DL directly connected to the anode electrode of the OLED. Advantages of obtaining the sensing voltage through the current path as in the first embodiment are as follows.

[0068] Since the sensing operation must be performed for each pixel, each pixel must be connected to the ADC through a vertical line such as the data line DL.

[0069] Since the pixel circuit for internal compensation of a conventional organic light emitting display device writes a data voltage to the gate electrode or the source electrode of the driving transistor DT, the data line DL is connected to the gate electrode or the source electrode of the driving transistor. Therefore, in the conventional organic light emitting display device, the driving transistor DT is located between the data line DL and the anode electrode of the OLED.

[0070] In a conventional method of obtaining the anode voltage of the OLED, the shortest path between the anode electrode of the OLED and the data line DL sequentially passes through the driving transistor DT, the second transistor T2 and the data line DL. However, the driving transistor DT is arranged in this sensing path. When the voltage of the anode electrode of the OLED is sensed by the current path passing through the driving transistor DT, the threshold voltage of the driving transistor DT affects the sensing voltage. That is, sensing accuracy is lowered.

[0071] Therefore, a path is required to bypass the driving transistor DT to connect the anode electrode of the OLED and the data line DL. Thus, there is a disadvantage that additional switching elements and conductive patterns are required to use the bypass path.

[0072] A method of connecting a vertical line other than the data line, for example, the initialization line to the anode electrode of the driving transistor DT and acquiring the sensing voltage through the initialization line can be used in a method that does not use the bypass path. However, in addition to the high potential voltage line supplying the high potential voltage VDD and the data line DL, arranging the initialization line as vertical lines increases the vertical width of the pixels, which is very disadvantageous for realizing high resolution.

[0073] On the other hand, the organic light emitting display device according to the first embodiment can perform the sensing operation using only the configuration of the

internal compensation circuit which is necessary during the displaying period, without requiring additional patterns and switch elements.

[0074] In addition, according to the first embodiment of the present disclosure, since the sensing voltage is obtained by using the data line DL, the initialization line can be arranged as a horizontal line. Since a longitudinal width is wider than a lateral width in the shape of the pixel, the design margin is larger when the initialization line is arranged as the horizontal line, which is advantageous for realizing high resolution.

[0075] In order to drive the pixels arranged in the n-th pixel line in the first embodiment, three scan signals, namely, the (n-2)-th scan signal SCAN(n-2), the (n-1)-th scan signal SCAN(n-1) and the n-th scan signal SCAN(n) are required. That is, in a general pixel array structure, three scan lines must be arranged in one pixel line. In order to reduce the number of scan lines arranged in a pixel line, the pixel array can have the following structure.

[0076] FIG. 7 is a schematic diagram of pixels according to the first embodiment of the present disclosure.

[0077] Referring to FIG. 7, in a (n-1)-th pixel line HL(n-1), a (n-1)-th emission line EML(n-1), a (n-1)-th scan line SL(n-1) and a (n-2)-th scan line SCAN(n-2) are sequentially arranged. In a n-th pixel line HL(n), a n-th emission line EML(n), a n-th scan line SL(n) and the (n-1)-th scan line SCAN(n-1) are sequentially arranged. The gate electrode of the sixth transistor T6 of the pixels arranged in the n-th pixel line HL(n) is connected to the (n-2)-th scan line SL(n-2) arranged at the lowermost end of the (n-1)-th pixel line HL(n-1). As a result, the n-th pixel line HL(n) does not need to be arranged with the (n-2)-th scan line SL(n-2), which makes it easy to design a pixel structure.

[0078] FIG. 8 is a diagram showing an array structure of pixels according to a second embodiment of the present disclosure, and FIG. 9 is a diagram showing a pixel circuit according to the second embodiment. These configurations of the pixels of FIGS. 8 and 9 can be used in the display device of FIG. 1 or other suitable display devices.

[0079] Referring to FIGS. 8 and 9, first through third pixels P1, P2, and P3 representing R, G, and B colors share a compensation node STR. A voltage drop compensation unit STRC controls the compensation node STR to compensate for the voltage drop of the high potential voltage VDD between the pixel lines.

[0080] Each of the first through third pixels P1, P2, and P3 includes a driving transistor DT, first to sixth transistors T1 to T6, and a storage capacitor Cst.

[0081] The driving transistor DT controls the driving current applied to the OLED according to its source-gate voltage Vsg. In the driving transistor DT, a gate electrode is connected to a first node N1, a drain electrode is connected to a second node N2, and a source electrode is connected to the input terminal of a high potential voltage VDD.

[0082] The first transistor T1 includes a gate electrode connected to an n-th scan line SL(n), a source electrode connected to a third node N3, and a drain electrode connected to the first node N1. The first transistor T1 connects the gate electrode and the drain electrode of the driving transistor DT in response to an n-th scan signal SCAN(n).

[0083] A second transistor T2 includes a gate electrode connected to the n-th scan line SL(n), a source electrode connected to the data line DL, and a drain electrode connected to the second node N2. The second transistor T2

connects the data line DL and the second node N2 in response to the n-th scan signal SCAN(n).

[0084] A third transistor includes a gate electrode connected to the n-th emission line EML(n), a source electrode connected to the input terminal of the high potential voltage VDD, and a drain electrode connected to the third node N3. The third transistor T3 applies the high potential voltage VDD to the third node N3 in response to the n-th emission signal EM(n).

[0085] A fourth transistor includes a gate electrode connected to an n-th emission line EML(n), a source electrode connected to the second node N2, and a drain electrode connected to an anode electrode of the OLED. The fourth transistor T4 connects the anode electrode of the OLED with the second node N2 in response to the n-th emission signal EM(n).

[0086] A fifth transistor includes a gate electrode connected to an (n-1)-th scan line SL(n-1), a source connected to the first node N1, and a drain electrode connected to the initialization line VIL. The fifth transistor T5 applies the initialization voltage Vini to the first node N1 in response to an (n-1)-th scan signal SCAN(n-1).

[0087] A sixth transistor includes a gate electrode connected to an (n-2)-th scan line SL(n-2), a source connected to the anode of the OLED, and a drain electrode connected to an initialization line VIL. The sixth transistor T6 applies an initialization voltage Vini to the anode of the OLED in response to an (n-2)-th scan signal SCAN(n-2).

[0088] The storage capacitor Cst is connected between the first node N1 and the compensation node STR.

[0089] The voltage drop compensation unit STRC includes first to third compensation transistors Tc1, Tc2 and Tc3.

[0090] The first compensation transistor Tc1 includes a gate electrode connected to the n-th emission line EML(n), a source electrode connected to the input terminal of the high potential voltage VDD, and a drain electrode connected to the compensation node STR. The first compensation transistor Tc1 applies the high potential voltage VDD to the compensation node STR in response to the n-th emission signal EM(n).

[0091] The second compensation transistor Tc2 includes a gate electrode connected to the (n-1)-th scan line SL(n-1), a source electrode connected to the compensation node STR, and a drain electrode connected to an input terminal of a reference voltage Vref. The second compensation transistor Tc2 applies the reference voltage Vref to the compensation node STR in response to the (n-1)-th scan signal SCAN(n-1).

[0092] The third compensation transistor Tc3 includes a gate electrode connected to the n-th scan line SL(n), a source electrode connected to the compensation node STR, and a drain electrode connected to an input terminal of a reference voltage Vref. The third compensation transistor Tc3 applies the reference voltage Vref to the compensation node STR in response to the n-th scan signal SCAN(n).

[0093] The pixel circuit according to the second embodiment compensates the change of the threshold voltage of the driving transistor DT in real time within the displaying period according to the internal compensation scheme.

[0094] FIG. 10 is a diagram illustrating the timings of gate signals in the displaying period according to the second embodiment, and FIGS. 11A to 11D are equivalent circuit diagrams of pixels in a first initialization period, a second

initialization period, a sampling period, and a light emission period, respectively. Hereinafter, in the second embodiment, the same reference numerals and names are used for components substantially the same as those in the first embodiment described above.

[0095] Referring to FIGS. 8 to 11D, the operations of the pixel are as follows which emits light while compensating for the threshold voltage change of the driving transistor in real time.

[0096] Referring to FIGS. 8 to 10 and 11A, in the first initialization period Ti1, the (n-2)-th scan signal SCAN(n-2) maintains a turn-on voltage. The sixth transistor T6 applies the initialization voltage Vini to the anode of the OLED in response to the (n-2)-th scan signal SCAN(n-2). As a result, the anode of the OLED is initialized to the initialization voltage Vini in the first initializing period Ti1. The initialization voltage Vini is selected within a voltage range sufficiently lower than the operation voltage of the OLED and can be set to be equal to or lower than the low potential voltage ELVSS.

[0097] Referring to FIGS. 8 to 10 and 11B, the (n-1)-th scan signal SCAN(n-1) maintains the turn-on voltage in the second initialization period Ti2. The fifth transistor T5 applies the initialization voltage Vini to the first node N1 in response to the (n-1)-th scan signal SCAN(n-1). In the second initializing period Ti2, the first node N1 is initialized to the initialization voltage Vini. The second compensation transistor Tc2 applies the reference voltage Vref to the compensation node STR in response to the (n-1)-th scan signal SCAN(n-1). The reference voltage Vref can be set to a voltage lower than the high potential voltage VDD.

[0098] Referring to FIGS. 8 to 10 and 11C, in the sampling period Ts, the n-th scan signal SCAN(n) maintains the turn-on voltage. The first transistor T1 connects the first node N1 and the third node N3 in response to the n-th scan signal SCAN(n). The second transistor T2 writes a data voltage Vdata to the second node N2 in response to the n-th scan signal SCAN(n). A current flows between the drain and source electrodes of the driving transistor DT in the sampling period Ts, and this current flows until the voltage of the source electrode is saturated to the magnitude of the sum ($V_{data} + V_{th}$) of the data voltage Vdata and the threshold voltage Vth of the driving transistor DT. That is, during the sampling period Ts, the gate electrode of the driving transistor DT is sampled with a magnitude of ($V_{data} + V_{th}$).

[0099] The third compensation transistor Tc3 applies the reference voltage Vref to the compensation node STR in response to the n-th scan signal SCAN(n).

[0100] Referring to FIGS. 8 to 10 and 11D, the n-th emission signal EM(n) maintains the turn-on voltage in the emission period Te after a holding period Td. The third transistor T3 and the fourth transistor T4 are turned on in response to the n-th emission signal EM(n), and as a result, a current is generated from the input terminal of the high potential voltage VDD to the anode of the OLED depending on the voltage set between the gate and the source of the driving transistor DT.

[0101] The first compensation transistor Tc1 applies the high potential voltage VDD to the compensation node STR in response to the n-th emission signal EM(n).

[0102] Since the compensation node STR is charged with the reference voltage Vref in the sampling period Ts, in the emission period Te the voltage of the compensation node STR rises by the magnitude of ($VDD - Vref$) in comparison

with the sampling period T_s . Since the voltage change amount of the compensation node STR is reflected to the first node N1 by coupling phenomenon, a voltage change of an amount of $(V_{DD}-V_{ref})$ occurs in the first node N1. That is, the voltage of the first node N1 becomes $(V_{data}+V_{th}+V_{DD}-V_{ref})$ in the emission period T_e from $(V_{data}+V_{th})$ in the sampling period T_s .

[0103] As a result, the driving current I_{oled} flowing in the OLED in the emission period T_e is expressed by the following Equation 2.

$$I_{OLED}=k/2\{(V_{gs}-V_{th})\}^2=k/2\{(V_g-V_s-V_{th})\}^2=k/2\{(V_{data}+V_{th}+V_{DD}-V_{ref})-V_{DD}-V_{th}\}^2=k/2\{(V_{data}-V_{ref})\}^2 \quad \text{Equation 2}$$

[0104] At this time, since $V_{th}<0$, Equation 2 becomes $k/2\{(V_{data}-V_{DD})\}^2$.

[0105] In Equation 2, k represents a proportional constant determined by electron mobility, parasitic capacitance, and channel capacitance of the driving transistor DT, and the like. As a result, during the light emission period T_e , the driving current flowing through the OLED is not affected by the threshold voltage V_{th} of the driving transistor DT.

[0106] The pixel circuit according to the first embodiment compensates for the threshold voltage deviation of the OLED within the sensing period, similar to the first embodiment. The method of sensing the anode voltage of the organic light emitting diode in the second embodiment can be the same as that of the first embodiment.

[0107] As a result, the organic light emitting diode display device according to the second embodiment does not require additional patterns and switch elements and can perform a sensing operation using only the configuration of an internal compensation circuit necessary during a displaying period. Since a sensing voltage is obtained by using a data line, an initialization line can be disposed as a horizontal line. Since a longitudinal width is wider than a lateral width in the shape of the pixel, the design margin is larger when the initialization line is arranged as the horizontal line, which is advantageous for realizing high resolution.

[0108] Throughout the description, it should be understood by those skilled in the art that various changes and modifications are possible without departing from the technical principles of the present disclosure. Therefore, the technical scope of the present disclosure is not limited to the detailed descriptions in this specification but should be defined by the scope of the appended claims.

What is claimed is:

1. An organic light emitting display device, comprising: an organic light emitting diode (OLED); a driving transistor connected to an anode electrode of the OLED; a scan transistor connected to the anode electrode of the OLED and a data line; a digital-to-analog converter (DAC) configured to supply a data voltage for displaying to the data line in a displaying period, and supply a data voltage for sensing to the data line in a sensing period; and a sensing unit configured to obtain an anode voltage of the OLED as a sensing voltage through the data line in the sensing period.
2. The organic light emitting display device of claim 1, further comprising: a first switch connected between the data line and the DAC, and turned on during a first period within the sensing period; and

a second switch connected between the data line and the sensing unit, and turned on during a second period following the first period within the sensing period.

3. The organic light emitting display device of claim 2, wherein a scan signal maintains a turn-on voltage within the sensing period.

4. The organic light emitting display device of claim 2, further comprising:

an emission control transistor connected between a source electrode of the driving transistor and the anode electrode of the OLED,

wherein the data line is connected to the anode electrode of the OLED through the scan transistor and the emission control transistor.

5. An organic light emitting display device, comprising: pixels connected to a data line and a scan line,

wherein an n -th pixel disposed on an n -th pixel line, n being an integer, comprises:

a driving transistor including a gate electrode connected to a first node, a drain electrode connected to a second node and a source electrode connected to a third node;

an organic light emitting diode (OLED) connected to the second node;

a first transistor connected between the first node and the second node;

a scan transistor connected between the data line and the second node; and

a first emission control transistor connected between the second node and the OLED.

6. The organic light emitting display device of claim 5, wherein, during a sampling period, the scan transistor of the n -th pixel applies a data voltage provided through the data line to the second node in response to an n -th scan signal, and the first transistor of the n -th pixel connects the first node and the third node in response to the n -th scan signal.

7. The organic light emitting display device of claim 6, wherein the n -th pixel further comprises a second emission control transistor connected between an input terminal of a high potential voltage and the third node, and

wherein, during an emission period following the sampling period, the first emission control transistor of the n -th pixel connects the input terminal of the high potential voltage and the third node in response to an n -th emission signal, and the second emission control transistor of the n -th pixel connects the second node and an anode electrode of the OLED in response to the n -th emission signal.

8. The organic light emitting display device of claim 6, wherein the n -th pixel further comprises a first initialization transistor connected between an initialization line and an anode electrode of the OLED, and

wherein the first initialization transistor of the n -th pixel applies an initialization voltage from the initialization line to anode electrode of the OLED in response to an $(n-2)$ -th scan signal, during a first initialization period before the sampling period,

9. The organic light emitting display device of claim 8, wherein the $(n-2)$ -th scan signal turns on a scan transistor disposed on an $(n-2)$ -th pixel line.

10. The organic light emitting display device of claim 8, wherein the n -th pixel further comprises a second initialization transistor connected between the initialization line and the first node, and

wherein the second initialization transistor of the n-th pixel applies the initialization voltage to the first node in response to an (n-1)-th scan signal, during a second initialization period following the first initialization period.

11. The organic light emitting display device of claim **10**, wherein the (n-1)-th scan signal turns on a scan transistor disposed on an (n-1)-th pixel line.

12. The organic light emitting display device of claim **11**, wherein a second initialization transistor of a pixel disposed on the (n-1)th pixel line is provided with the (n-1) scan signal through an (n-1)-th scan line, and

wherein a gate electrode of the first initialization transistor of the n-th pixel is connected to the (n-1)-th scan line disposed on the (n-1)-th pixel line.

13. The organic light emitting display device of claim **5**, wherein the n-th pixel further comprises a capacitor including a first electrode connected to the input terminal of the high potential voltage and a second electrode of first node.

14. The organic light emitting display device of claim **13**, wherein the n-th pixel comprises:

a first compensation transistor connected between the first electrode of the capacitor and the input terminal of the high potential voltage;

a second compensation transistor connected between the first electrode of the capacitor and an input terminal of the (n-1)th scan signal; and

a third compensation transistor connected between the first electrode of the capacitor and an input terminal of the n-th scan signal.

15. The organic light emitting display device of claim **5**, further comprising:

a digital-to-analog converter (DAC) configured to supply a data voltage for displaying to the data line in a displaying period, and supply a data voltage for sensing to the data line in a sensing period; and

a sensing unit configured to obtain an anode voltage of the OLED as a sensing voltage through the data line in the sensing period.

16. The organic light emitting display device of claim **15**, further comprising:

a first switch connected between the data line and the DAC, and turned on during a first period within the sensing period; and

a second switch connected between the data line and the sensing unit, and turned on during a second period following the first period within the sensing period.

* * * * *

专利名称(译)	有机发光显示装置		
公开(公告)号	US20200152130A1	公开(公告)日	2020-05-14
申请号	US16/681619	申请日	2019-11-12
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	HONG SOONHWAN LEE CHEOLHWAN		
发明人	HONG, SOONHWAN LEE, CHEOLHWAN		
IPC分类号	G09G3/3258 G09G3/3233 G09G3/3275 H01L27/32		
CPC分类号	H01L27/3248 G09G2320/045 G09G2320/0233 G09G3/3275 G09G2300/0426 H01L27/124 G09G3/3233 G09G3/3258 G09G2310/027 H01L27/3276 G09G2300/0809 G09G2300/0819 G09G2300/0842 G09G2300/0861 G09G2310/0256 G09G2320/0238 G09G2320/0295		
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摘要(译)

有机发光显示装置可以包括有机发光二极管 (OLED) , 连接至OLED的阳极的驱动晶体管, 扫描晶体管, 数模转换器 (DAC) 和感测单元。扫描晶体管连接到OLED的阳极和数据线。 DAC在显示时段中向数据线提供用于显示的数据电压, 并且在感测时段中向数据线进行感测的数据电压。感测单元在感测时段中通过数据线获得OLED的阳极电压作为感测电压。

